DC to 400MHz, 92 dB Logarithmic Amplifier

Features

- Demodulating Logarithmic Amplifier
- 92dB Dynamic Range: -88dBV to +4dBV
- DC to 400MHz Operation, ±1dB Linearity
- Fast Voltage Mode Output, t_R < 30ns
- High Output Current Drive
- Slope of +24mV/dB, Intercept of -108dBV
- Highly Stable Scaling Over Temperature
- Fully Differential DC-Coupled Signal Path
- Single Supply Operation: 3.0V to 5.5V
- Low Quiescent Current:
  - 5.2mA Operation Mode
  - < 0.1uA Disable Mode
- Extended Temperature Ranges
  From -40°C to +125°C
- Green Small Packaging: MSOP-8

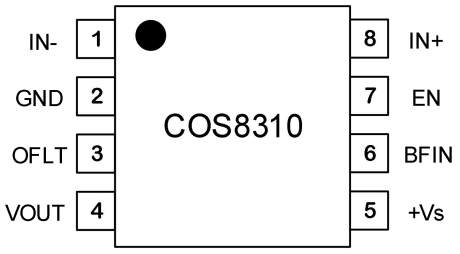
Applications

- Receiver Signal Strength Indication (RSSI)
- Transmitter Antenna Power Measurement
- Radar and Sonar Signal Processing
- Conversion of Signal Level to dB form

General Description

The COS8310 is a DC to 400MHz, multistage demodulating logarithmic amplifier (log amp) for use in receiver signal strength indication (RSSI). It uses the successive detection technique to achieve a dynamic range of up to 92dB. The demodulated output is accurately scaled, with a log slope of 24mV/dB and an intercept of -108 dBV. The scaling parameters are supply and temperature independent.

The COS8310 is capable of driving up to 25mA current into a grounded load in under 30ns. It is easy to use, requiring no significant external components. A single supply voltage of 3.0V to 5.5V at 5.2mA is needed, corresponding to a power consumption about 25 mW at 5V. The COS8310 can be enabled or disabled by a CMOS/TTL compatible level at EN (pin 7).



Pin Diagram

Rev1.0

Copyright@2018 Cosine Nanoelectronics Inc. All rights reserved

The information provided here is believed to be accurate and reliable. Cosine Nanoelectronics assumes no reliability for inaccuracies and omissions. Specifications described and contained here are subjected to change without notice on the purpose of improving the design and performance. All of this information described herein should not be implied or granted for any third party.

1. Block Diagram and Pin Functions

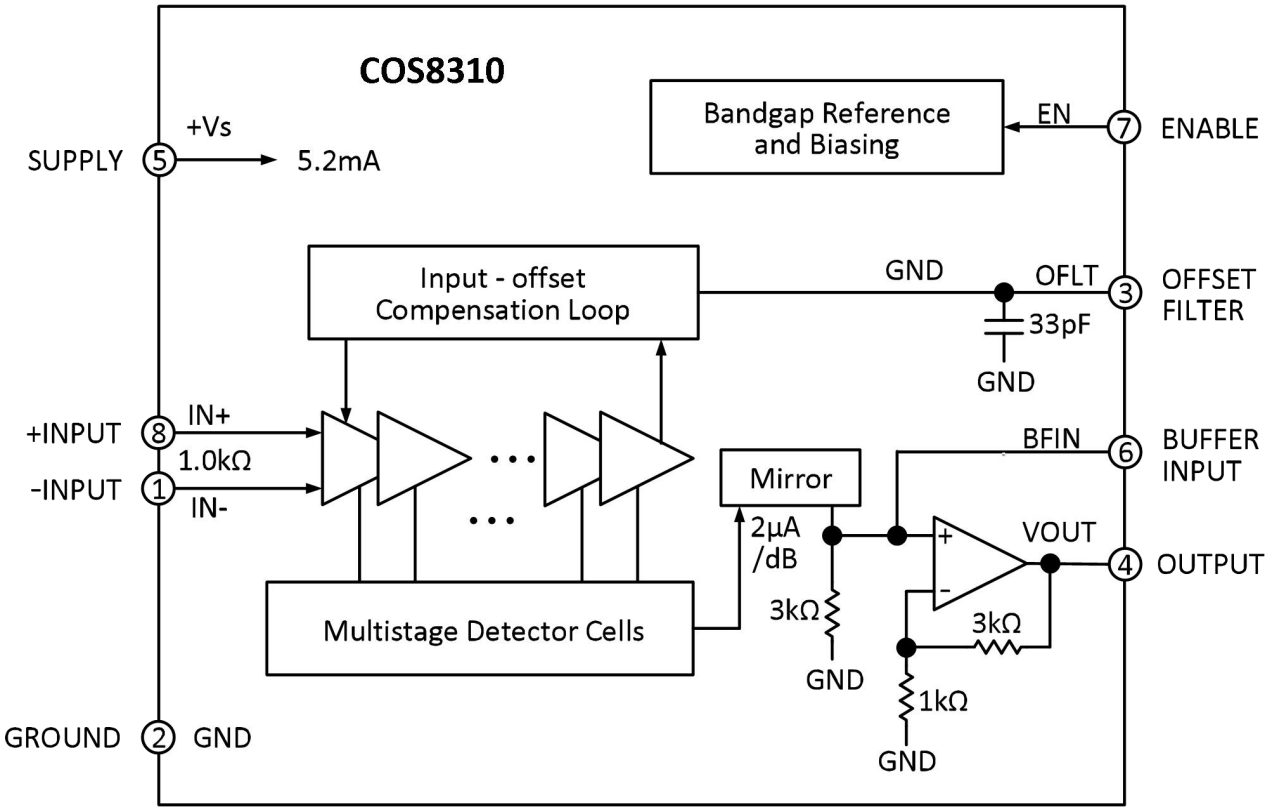


Figure 1. Block Diagram

Pin Description

Pin No.	Pin Name	Description
1	IN-	One of Amplifier Inputs. Internally Biased.
2	GND	Amplifier Ground.
3	OFLT	Offset Filter Access. An External Capacitor on OFLT Pin Lowers the High-Pass Corner
4	VOUT	Amplifier Low Impedance Voltage Output.
5	+Vs	Positive Power Supply, 3.0V to 5.5V at 5.2mA Quiescent Current.
6	BFIN	Buffer Input. Used to Lower Post-detection Bandwidth.
7	EN	Chip Enable. Active when High
8	IN+	Second of Amplifier Inputs. Internally Biased.

2. Product Specification

2.1 Absolute Maximum Ratings (1,2)

Parameter	Rating	Units
Power Supply: +Vs	+6.0	V
Input Power, Single-Ended (50Ω)	18	dBm
Input Power, Differential Drive	21	dBm
Internal Power Dissipation	200	mW
Storage Temperature Range	-65 to 150	°C
Junction Temperature	150	°C
Operating Temperature Range	-40 to 125	°C
ESD Susceptibility, HBM	4000	V

(1) Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

2.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance, $R_{\theta JA}$ (Juntion-to-Ambient)	200 (MSOP8)	°C/W

2.3 Recommended Operating Conditions

Parameter	Rating	Unit
DC Supply Voltage, Vs	+3.0 to +5.0	V
Input Power	-75 to +17	dBm
Operating Ambient Temperature	-40 to +85	°C

2.4 Electrical Characteristics

(T_A=+25°C, V_S = +5V, unless otherwise noted)

Parameter	Sym.	Conditions	Min	Typ	Max	Unit
Input Characteristics (IN+, IN-)						
Maximum Input		Single-ended, p-p		± 2.2		V
		Specified in dBV		4		dBV
		Equivalent Power in 50Ω		17		dBm
		Differential drive, p-p		20		dBm
Input Resistance	R_{IN}		0.9	1.1	1.3	kΩ
Input Capacitance	C_{IN}			1.5		pF
DC Bias Voltage		Either Input, Internal Bias		2.5		V
Noise Floor	e_n	Terminated 50Ω source		2.0		nV/ √Hz
Equivalent Noise Power		400MHz bandwidth, in 50Ω		-75		dBm
Output Characteristics (VOUT)						
±3dB Error Dynamic Range		From noise floor to maximum input		92		dB
Transfer Slope		10MHz ≤ f ≤ 200MHz	22	24	26	mV/dB
		−40°C ≤ T_A ≤ +85°C	20		26	mV/dB
Log Offset (Intercept), 10 MHz≤f≤100 MHz		T_A= +25°C	-115	-108	-99	dBV
		−40°C ≤ T_A ≤ +85°C	-120	-95	-86	dBV
		Equivalent dBm (50Ω), T_A=+25°C	-102	-95	-86	dBm
		Equivalent dBm (50Ω), −40°C ≤ T_A ≤ +85°C	-107		-83	dBm
		Temperature sensitivity		-0.05		dB/°C
Linearity Error (Ripple)		Input from -88dBV (-75dBm) to +2dBV (+15dBm)		±1		dB
Output Voltage		Input = -88dBV (-75dBm)		0.5		V
		Input = 4 dBV (17dBm)		2.75		V
Maximum Sink Current	I_{SK}		25			mA
Output Impedance	Z_{OUT}			0.05		Ω
Minimum Load Resistance	R_L			100		Ω

Video Bandwidth				15		MHz
Rise Time (10% to 90%)	t_R	Input level = -43dBV, RL≥500Ω, CL ≤ 50pF		30		ns
		Input level = -3dBV, RL≥500Ω, CL ≤ 50pF		40		ns
Fall Time (10% to 90%)	t_F	Input level = -43dBV, RL≥500Ω, CL ≤ 50pF		30		ns
		Input level = -3dBV, RL≥500Ω, CL ≤ 50pF		40		ns
Output Settling Time to 1%		Input level = -13dBV, RL≥500Ω, CL ≤ 50pF		50		ns
Power Supply (+Vs)						
Operating Voltage Range	V_S		3.0		5.5	V
Quiescent Current / Amplifier	I_Q		4.2	5.2	6.2	mA
		−40°C ≤ T_A≤ +85°C	4.5	5.5	6.5	mA
Disable Current	I_{pd}				0.1	μA
Logic Level to Enable Power		High condition, −40°C ≤ T_A≤ +85°C		2.4		V
Logic Level to Disable Power		Low condition, −40°C ≤ T_A≤ +85°C		0.8		V
Input Current When High		3V at EN		15		μA

2.5 Typical Performance Characteristics

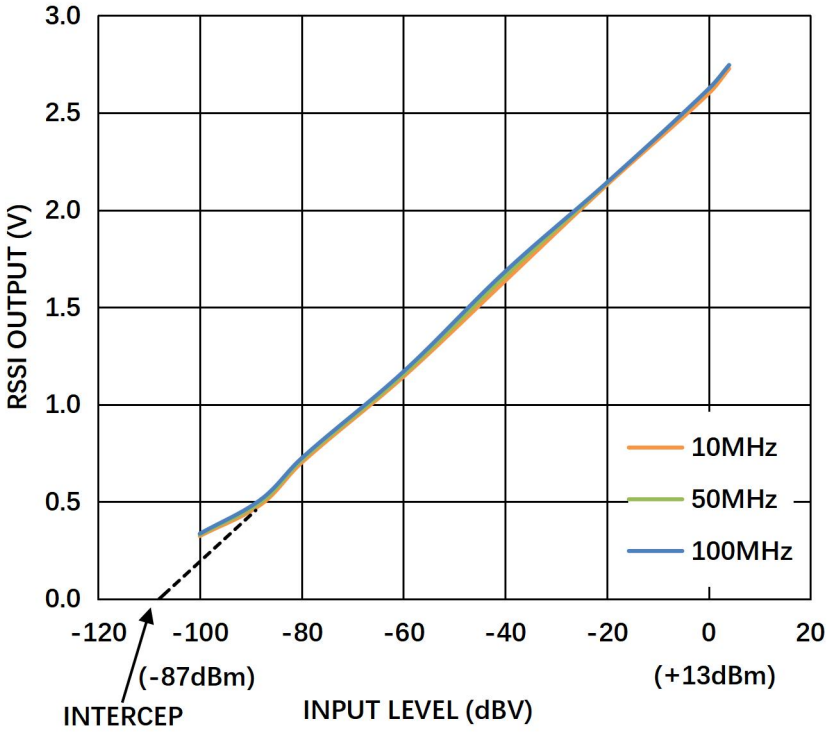


Figure 2. RSSI Output vs. Input Level for Sine Inputs at T_A=25°C for Frequencies of 10MHz, 50MHz, and 100MHz

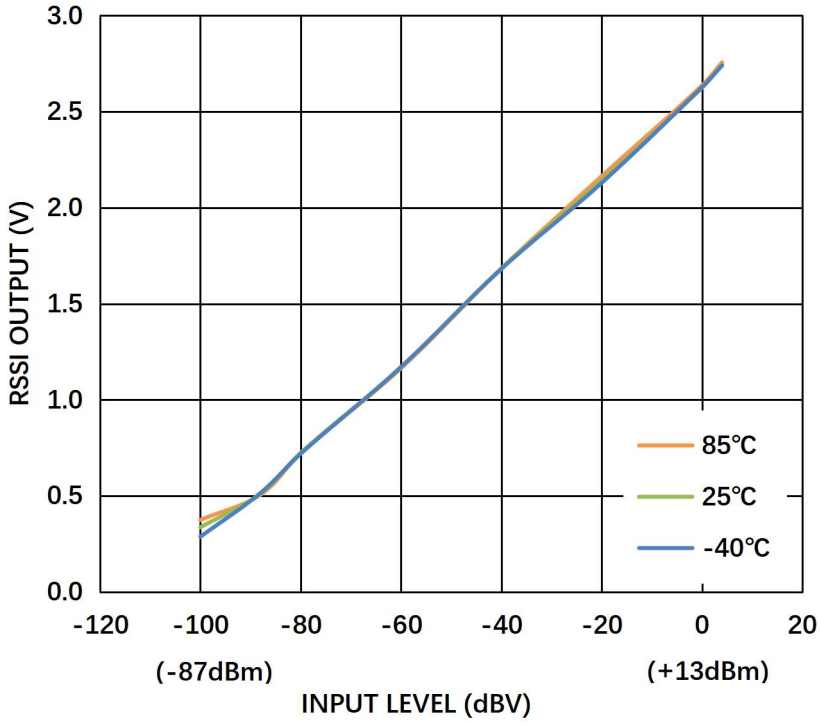


Figure 3. RSSI Output vs. Input Level for Sine Inputs at 100MHz at T_A=-40°C, +25°C, and +85°C

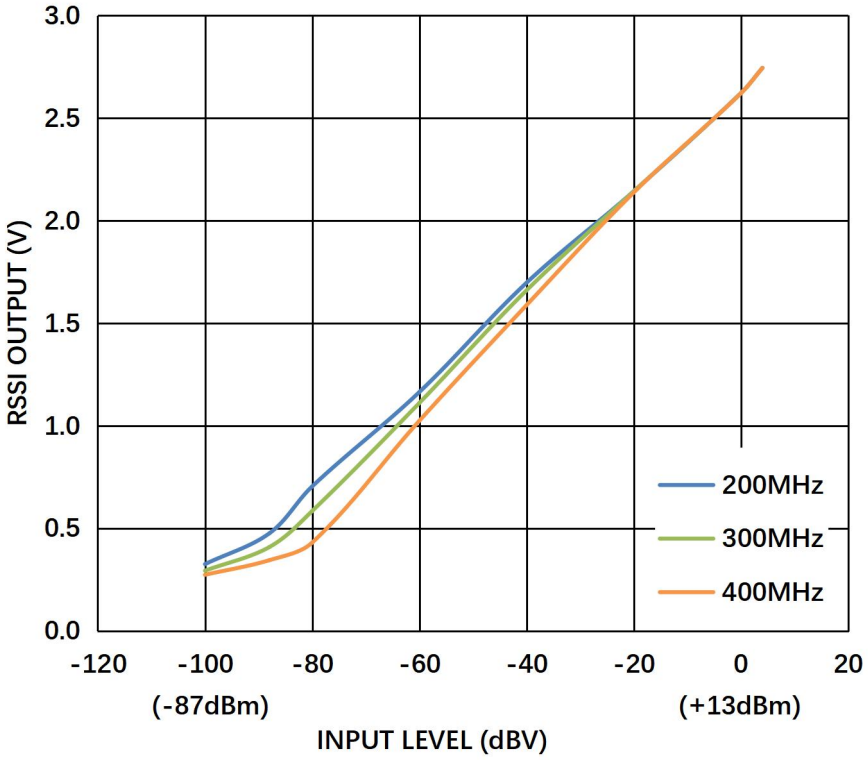


Figure 4. RSSI Output vs. Input Level for Sine Inputs at T_A=25°C for Frequencies of 200MHz, 300MHz, and 400MHz

3.0 Application Notes

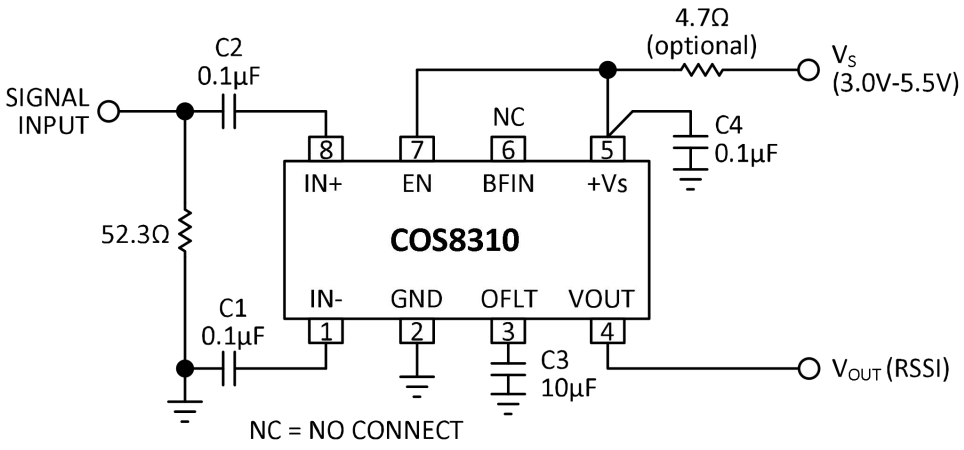


Figure 5. Basic Connections

Input Matching (PIN: IN+, IN-)

Figure 5 shows the basic connections needed for most applications. While the COS8310's input can be driven differentially, the input signal is, in general, single-ended. C1 is tied to ground, and the input signal is coupled in through C2. Capacitor C1 and C2 should have the same value to minimize start-up transients when the enable feature is used; otherwise, their values need not be equal.

The 52.3 Ω resistor combines with 1.1 kΩ input impedance of the COS8310 to yield a simple broadband 50 Ω input match. The C1/C2 and input resistor form a high pass filter with corner f_{HP}= 1/(π × 50 × C_C), where C1=C2=C_C. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low-pass filter should be added at the input for similar reasons. This should generally be placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

Output Filtering (PIN: BFIN)

For applications in which maximum video bandwidth and, consequently, fast rise time are desired, it is essential that the BFIN pin be left unconnected and free of any stray capacitance. The nominal output video bandwidth of 15 MHz can be reduced by connecting a ground-referenced capacitor (C_{FILT}) to the BFIN pin. This is generally done to reduce output ripple (at twice the input frequency for a symmetric input waveform such as sinusoidal signals).

C_{FILT} is selected using the following equation:

$$C_{FILT} = \frac{1}{(2\,\pi \times 3\text{k}\Omega \times \text{VideoBandwidth})} - 2.1\text{pF}$$

The video bandwidth should typically be set at a frequency equal to about one-tenth the minimum input frequency. This ensures that the output ripple of the demodulated log output, which is at twice the input frequency, is well filtered. For example, for a video bandwidth of 1MHz, the C_{FILT} is approximately 50pF.

Lowering the High-Pass Corner Frequency of the Offset Compensation Loop (PIN: OFLT)

In normal operation using an ac-coupled input signal, the OFLT pin can be left unconnected. Input-referred dc offsets of about 1.5 mV in the signal path are nulled via an internal offset control loop. This loop has a high-pass −3 dB corner at about 6 MHz. In low frequency ac-coupled applications, it is necessary to lower this corner frequency to prevent input signals from being misinterpreted as offsets. An external capacitor on OFLT Pin lowers the high-pass corner to arbitrarily low frequencies. For example, by using a 10μF capacitor, the 3 dB corner is reduced to 6kHz. The corner frequency is set by the following equation:

$$f_{HP} = \frac{1}{(2\pi \times 2.65 \times C_{OFLT})}$$

where C_{OFLT} is the capacitor connected to OFLT.

Output vs. Input Level

Figure 2 shows the output vs. the input level for sine inputs at the 10MHz, 50MHz, and 100MHz. The transfer function of the COS8310 can be characterized in terms of its slope (V_{SLOPE}) and intercept (P_{INT}). The logarithmic slope (V_{SLOPE}) is defined as the change in the RSSI output voltage for a 1dB change at the input. For the COS8310, slope is nominally 24mV/dB. Therefore, a 10dB change at the input results in a change at the output of approximately 240mV. The dynamic range of the log amp is defined as the range over which the slope remains within a certain error band, usually ±1dB or ±3dB. The intercept is the point at which the extrapolated linear response would intersect the horizontal axis (see Figure 2). For the COS8310, the intercept is calibrated to be −108 dBV (−95 dBm). Using the slope and intercept, the output voltage can be calculated for any input level within the specified input range using the following equation:

$$V_{OUT} = V_{SLOPE}\,(P_{IN} - P_{int})$$

Where P_{IN} is the input signal expressed in dB relative to some reference level (either dBm or dBV in this case). For example, for an input level of −33 dBV (−20 dBm), the output voltage is $V_{OUT} = V_{SLOPE}\,(P_{IN} - P_{int})$ = 0.024 V/dB × (−33 dBV − (−108 dBV)) = 1.8 V

Since waveforms is also involved in the response of a log amp, which, for a complex input such as a CDMA signal, does not follow the rms value exactly, a correction factor should be add to the measured input level as shown in the following Table.

Correction for Signals with Differing Crest Factors

Signal Type	Correction Factor (dB)
Sine wave	0
Square wave or dc	-3.01
Triangular wave	0.9
GSM channel (all time slots on)	0.55
CDMA channel (forward link, nine channels on)	3.55
CDMA channel (reverse link)	0.5
PDC channel (all time slots on)	0.58

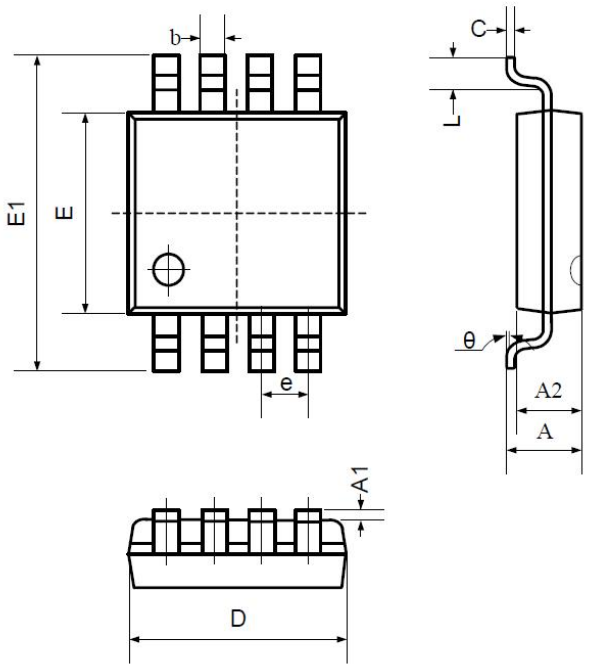
Power-Supply Bypassing and Layout

The COS8310 operates from a single +3V to +5.5V supply or dual ±1.5V to ±2.75V supplies. For single-supply operation, bypass the power supply +Vs with a 0.1μF ceramic capacitor which should be placed close to the +Vs pin. For dual-supply operation, both the +Vs and the -Vs supplies should be bypassed to ground with separate 0.1μF ceramic capacitors. 2.2μF tantalum capacitor can be added for better performance. Optionally, a small series resistor can be placed in the power line to give additional filtering of power-supply noise.

The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high frequency impedance of the path. High speed currents in an inductive ground return create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance. Thus a ground plane layer is important for high speed circuit design.

4. Package Information

4.1 MSOP8 (Package Outline Dimensions)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.200	0.031	0.047
A1	0.000	0.200	0.000	0.008
A2	0.760	0.970	0.030	0.038
b	0.30 TYP		0.012 TYP	
c	0.15 TYP		0.006 TYP	
D	2.900	3.100	0.114	0.122
e	0.65 TYP		0.026 TYP	
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
L	0.410	0.650	0.016	0.026
θ	0°	6°	0°	6°

5. Ordering Information

Model	Package	Order Number	Package Option	Marking Information
COS8310ARM	MSOP-8	COS8310ARM	Tape and Reel, 3000	COS8310

6. Related Parts

Part Number	Description
COS8042	170MHz, 6.1mA, High Speed Op Amps, 3.2V to 12V Supply
COS2172	10MHz, 1.2mA, RRIO Op Amps, 4.5 to 40V Supply
COS2333	350kHz, 18μA, Precision Op Amps, 1.8 to 5.5V Supply, Zero Drift, Vos<10μV
COS8552	1.5MHz, 55μA, Precision Op Amps, 1.8 to 5.5V Supply, Zero Drift, Vos<10μV
COS2388	9MHz, 570μA, Precision Op Amps, 1.8 to 5.5V Supply, Zero Drift, Vos<10μV
COS2227	10MHz, 1.3mA, Precision Op Amps, 4.5 to 36V Supply, Vos<50μV
COS2182	5MHz, 580μA, RRIO Precision Op Amps, 4.5 to 40V Supply, Vos<50μV
COS620	1.5MHz, 1.3mA, Instrumentation Amps, 4.5 to 36V Supply, Vos<50μV
COSINA333	150kHz, 65μA, Instrumentation Amps, 1.8 to 5.5V Supply, Vos<25μV